AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning on page 12, line 9, as follows:

In addition, the extension of the sidewalls 53 for defining the sidewall offsets 54 makes it possible to keep the source and drain diffusion layers 65 and 66 of NMOS and PMOS transistors 10 and 20 away from edges of the gate electrodes 52, and hence, to prevent generation of a leakage current between bands with the result of enhancement in a breakdown voltage between the source and drain diffusion layers. As shown in Figure 3, on either side of the gate electrode 52 in the NMOS and PMOS transistors 10 and 20, lateral dimensions of the heavily doped source and drain diffusion layers 65 and 66 disposed at the surface of the substrate are approximately equal to and aligned with lateral dimensions of the sidewall offsets 54.